Claims

[1] A method of manufacturing a contact portion, the method comprising:
forming a first signal line on a substrate;
forming an insulating layer covering the first signal line and having a contact hole exposing the first signal line;
forming a contact layer on the exposed surface of the first signal through the contact hole; and
forming a second signal line connected to the first signal line via the contact layer,
wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.

[2] The method of claim 1, wherein the substrate is soaked in chemical conversion solution including a conductive material to form the contact layer.

[3] The method of claim 2, wherein chemical conversion solution include at least one of W, Zr, Mo, and Cr.

[4] A method of manufacturing a thin film transistor array panel, the method comprising:
forming a gate line on a substrate;
forming a gate insulating layer;
forming a semiconductor layer;
forming an ohmic contact layer;
forming a data line and a drain electrode;
forming a passivation layer having a first contact hole exposing the portion of the drain electrode; and
forming a first contact layer on the exposed surface of the drain electrode through the first contact hole.

[5] The method of claim 4, wherein the substrate is soaked in chemical conversion solution including a conductive material to form the contact layer.

[6] The method of claim 5, wherein chemical conversion solution include at least one of W, Zr, Mo, and Cr.

[7] The method of claim 4, wherein a second contact hole exposing the end portion of the gate line or the data line is formed in the step of forming the passivation layer.

[8] The method of claim 7, wherein a second contact layer is formed on the exposed surface of the gate line or the data line through the second contact hole in the step of forming the first contact layer.

[9] The method of claim 4, further comprising a step of forming a storage electrode

line with the same layer as the gate line.

[10] The method of claim 8, wherein a second contact hole exposing the end portion of the storage electrode line is formed in the step of forming the passivation layer.

[11] The method of claim 9, wherein a second contact layer is formed on the exposed surface of the storage electrode line through the second contact hole in the step of forming the first contact layer.

[12] A contact portion comprising:
a substrate;
a first signal line formed on a substrate;
an insulating layer covering the first signal line and having a contact hole exposing the first signal line;
a contact layer on the exposed surface of the first signal through the contact hole; and
a second signal line formed on the insulating layer and connected to the first signal line via the contact layer,
wherein the first signal line is made of Al or Al alloy, and the second signal line is made of ITO or IZO.

[13] The contact portion of claim 12, wherein the contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.

[14] The contact portion of claim 12, further comprising a lower layer formed under the first signal line.

[15] The contact portion of claim 14, wherein the lower layer is a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.

[16] A thin film transistor array panel comprising:
a substrate;
a gate line formed on a substrate;
a gate insulating layer covering the gate line;
a semiconductor layer formed on the gate insulating layer;
a data line intersecting the gate line and having a source electrode overlapping the portion of the semiconductor layer;
a drain electrode overlapping the portion of the semiconductor layer;
a passivation layer covering the data line and the drain electrode, and having a first contact hole exposing the portion of the drain electrode;
a first contact layer formed on the exposed surface of the drain electrode through the first contact hole, and made of a conductive oxide layer; and
a pixel electrode formed on the passivation layer and connected to the drain electrode via the first contact layer.

[17] The panel of claim 16, further comprising a color filter formed on the data line and the drain electrode.

[18] The panel of claim 16, further comprising a storage electrode line formed with the same layer as the gate line.

[19] The panel of claim 18, wherein the storage electrode line includes Al and Al alloy.

[20] The panel of claim 18, wherein the passivation layer and the gate insulating layer have a second contact hole exposing the portion of the storage electrode line, further comprising a second contact layer formed on the exposed portion on the storage electrode line through the contact hole; and a contact assistant connected to the exposed portion of the storage electrode line via the second contact layer.

[21] The panel of claim 20, wherein the second contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.

[22] The panel of claim 16, wherein the passivation layer or the gate insulating layer have a third contact hole exposing the portion of the gate line or the data line, further comprising a third contact layer formed on the exposed portion on the gate line or the data line through the third contact hole; and a contact assistant connected to the exposed portion of the gate line or the data line via the third contact layer.

[23] The panel of claim 22, wherein the third contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.

[24] The panel of claim 16, further comprising an ohmic contact layer formed between the data line and the drain electrode, and the semiconductor layer.

[25] The panel of claim 24, wherein the ohmic contact layer has the same planar shape as the data line and the drain electrode, and the semiconductor layer has the planar shape as the data line and the drain electrode except for the channel portion between the drain electrode and the source electrode.

[26] The panel of claim 16, wherein the first contact layer include at least one of W, Zr, Mo, Cr, and an alloy including W, Zr, Mo, Cr.

[27] The panel of claim 16, wherein the gate line includes a conductive layer made of Al or Al alloy.

[28] The panel of claim 16, wherein the data line includes a first conductive layer made of Al or Al alloy.

[29] The panel of claim 28, wherein the data line further comprise a second conductive layer formed under the first conductive layer.

[30] The panel of claim 29, wherein the second conductive layer is made of a conductive layer including at least one of Cr, Ti, Mo, and MoW alloy.